UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,716	03/24/2004	Ian M. Davis	013098/GNRL/HMM	3729

7590 02/25/2008

Michael A. Bernadicou
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

EXAMINER	
SMITH, FRANCIS P	

ART UNIT	PAPER NUMBER
4151	

MAIL DATE	DELIVERY MODE
02/25/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/807,716	DAVIS ET AL.	
	Examiner	Art Unit	
	FRANCIS P. SMITH	4151	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/12/2004;4/25/2005;4/9/2007;2/4/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-4 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over He et al. (US 6,656,535 B2) in view of Takamasa et al (US 2004/0129294A1).

He teaches a method of fabricating a process chamber component comprising a ceramic form having grains and grain boundary regions. Regarding claim 1, He teaches an initial step of bead blasting the ceramic component to provide a textured and roughened surface (i.e. roughening the surface of the substrate to produce microfissures) col. 3, lines 45-65. Once the surface of the ceramic form has been treated by bead blasting, the surface may be further treated in a second treatment step by dipping or immersing the surface into a treatment solution to clean the surface of loose grains formed during the bead blasting process (i.e. treating the roughened surface to remove at least substantially all particles of the substrate material remaining on the roughened surface) (col. 4, lines 65-67; col. 5, lines 1-10). Once the ceramic form has been treated by dipping in the solution, a metal coating is formed over at least a portion of the ceramic form. The coating may comprise one or more metals that have substantial resistance to erosion, such as aluminum, titanium, copper, and chromium, and may be deposited by a plasma arc method (col. 5, lines 66-67; col. 6, lines 1-15). He does not disclose using a metal oxide.

As to claims 1,3,4, and 22, Takamasa teaches a structure cleaning and anticorrosion method whereby oxide films, such as zirconium oxide (i.e. a dielectric material as per claim 22), is formed on the surface of a base material by use of a high temperature plasma ([0016], lines 18-25). Therefore, it would have been obvious to one skilled in the art at the time of the invention to use Takamasa's zirconium oxide coating,

a dielectric material, on He's roughened surface in order to protect the substrate base by forming a protective coating.

Regarding claim 2, He teaches a chamber component (i.e. substrate) of ceramic form (col. 3, lines 26-27).

5. Claims 5-8, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over He et al. (US 6,656,535 B2) in view of Takamasa et al (US 2004/0129294A1), as applied to claim 1 above, and further in view of Huang (US 6,623,559B2) and Fortin (US 2003/0073307 A1).

He/Takamasa do not teach generating the plasma via a generating gas, generating the plasma in the presence of compressed air, or generating the plasma in a particular temperature range.

Huang discloses a method for producing compound semiconductor quantum particles that utilizes a plasma arc spray nozzle. The spray nozzle involves feeding a wire of metal or metal powders into the transferred arc, which rapidly fuses the metal for atomization. A large secondary flow of compressed air (i.e. generating the plasma in the presence of compressed air) functions to atomize the molten metal into the super-heated droplets. The plasma forming gas is introduced through a tube to the chamber, passing through a nozzle orifice. The ultra-high temperature in the plasma arc is typically between about 3000-57000°F (i.e. generating a plasma/applying the coating at a particular temperature). The resulting atomized, metal containing, airflow is directed into the chamber where semiconductor particles are formed (e.g. directing the plasma

toward surface to apply the coating composition to roughened surface) col. 13, lines 37-44; col. 14, lines 1-35. Huang does not disclose a particular plasma generating gas, hydrogen, nitrogen, argon, helium, and mixtures thereof.

Fortin teaches forming conductive layers on insulators by physical vapor deposition whereby argon is used as a plasma generating gas ([0002], lines 6-10). Therefore, it would have been obvious to one skilled in the art at the time of the invention to utilize the Huang's plasma generated by Fortin's argon in He/Takamasa's method in order to generate a plasma capable of coating the microfissures formed from the mechanical treatment.

6. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over He et al. (US 6,656,535 B2) in view of Takamasa et al (US 2004/0129294A1), as applied to claim 1 above, and further in view of Sugawara et al. (US 2004/0206388).

He, as modified by Takamasa, teaches a surface roughness of less then 150 microinches, but not a roughness of 180-320 microinches.

Sugawara teaches a method of manufacturing a photoelectric conversion device, whereby the surface of a semiconductor substrate is mechanically treated (i.e. sandblasted) to a roughness of approximately 200 microinches [0053]. Therefore, it would have been obvious to one skilled in the art at the time of the invention to obtain Sugawara's roughness on He/Takamasa's substrate in order to enhance the bonding between the substrate and subsequent coating layers.

7. Claims 11-13 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over He et al. (US 6,656,535 B2) in view of Takamasa et al (US 2004/0129294A1), as applied to claim 1 above, and further in view of Gorczyca et al. (US 2002/0094686A1).

For claims 11-13, He, as modified by Takamasa, teaches further treating the roughened surface by immersing the substrate in a treatment solution to clean said surface of loose grains formed during the bead blasting process (He: col. 4, lines 65-67; col. 5, lines 1-10). However, He/Takamasa does not disclose using a high concentration strong acid immersion bath.

Gorczyca teaches a semiconductor processing article that is prepared for use by mechanically blasting and chemically etching the surface of the article. After the roughening step, the substrate is subject to an etching solution (analogous to immersion bath) wherein the proportions of the acids in the solution can vary from 0-70 volume percent ([0028], lines 1-10). Therefore, it would have been obvious to one skilled in the art at the time of the invention to utilize Gorczyca's strong acid solution in He's immersion bath in order to effectively clean the substrate of debris to ensure the integrity of the semiconductor device.

Regarding claim 16-18, He/Takamasa do not disclose microfissures in the surface up to about 0.005 or 0.006 inches followed by filling/covering said microfissures.

Gorczyca teaches cracks forming in the substrate surface (i.e. microfissures) propagating from the surface into the substrate up to depths of 200 micrometers (i.e. 0.0078 inches). Then, a coating is applied over the surface to fill/cover the

microfissures. Therefore, it would have been obvious to one skilled in the art at the time of the invention to modify He/Takamasa's method by filling/covering Gorczyca's microfissures in the surface of the substrate in order to successfully support additional layers and to ensure the integrity of the semiconductor device.

For claim 19, He, as modified by Takamasa, discloses a coating thickness up to about 0.5mm (i.e. up to about 0.010 inches) (He: col. 6, lines 13-16).

8. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over He et al. (US 6,656,535 B2) in view of Takamasa et al (US 2004/0129294A1), Gorczyca et al. (US 2002/0094686A1), and further in view of Tarng et al (US 4,349,408).

He as modified by Takamasa and Gorczyca is silent regarding an immersion bath comprising of nitric acid and hydrofluoric acid.

Tarng discloses a method of depositing a refractory metal on a semiconductor substrate where the substrate is etched using a solution of nitric and hydrofluoric acid (col. 3, lines 25-32). Therefore, it would have been obvious to one skilled in the art at the time of the invention to employ Tarng's etching solution in He/Takamasa/Gorczyca's method in order to effectively remove unwanted species from the surface of the substrate.

9. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over He et al. (US 6,656,535 B2) in view of Takamasa et al (US 2004/0129294A1), Gorczyca et al. (US 2002/0094686A1), and further in view of Haerle et al. (US 6,565,667B2).

He as modified by Takamasa and Gorczyca does not disclose further cleaning the substrate after removal from the immersion bath.

Haerle teaches a process for cleaning ceramic articles whereby a substrate first undergoes a chemical stripping (analogous to the immersion bath), followed by a carbon dioxide cleaning (analogous to "cleaning the substrate) col. 3, lines 21-35. Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate Haerle's post bath cleaning step into He/Takamasa/Gorczyca's method in order to ensure all debris was removed from the surface of the substrate prior to further processing.

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1, 11,12, and 14 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1,4,6, and 10 of U.S. Patent No. 6,656,535 B2 (He et al.). Although the conflicting claims are not identical, they are not patentably distinct from each other because He teaches a method of fabricating a process chamber component that has a ceramic form with grains and grain boundary regions.

For claim 1, He claims bead blasting the component to provide a surface roughness average of less than about 150 micro inches, which is analogous to roughening the surface of the substrate material to produce microfissures therein. Then, the roughened surface is dipped into a solution having a concentration of acid or base that is sufficiently high to clean surface debris and contaminants off of the roughened surface, which is analogous to treating the roughened surface to remove at least substantially all particles of the substrate material remaining on the roughened surface. Lastly, a metal coating is formed over at least a portion of the ceramic form, which is analogous to coating the roughened surface with a coating composition containing at least one metal oxide (claims 1 and 10). Therefore, it would have been obvious to one skilled in the art at the time of the invention to utilize He's bead blasting, roughened substrate dipping, and metal coating (capable of forming an oxide in the presence of oxygen) in order to effectively clean and prepare a semiconductor substrate for further processing.

As for claims 11,12, and 14, He claims a solution comprising less than about 20 volume percent of one or more of KOH, HCL, or HNO_3 (Claim 4). Therefore, it

would have been obvious to one skilled in the art at the time of the invention to utilize He's acid bath combination to clean the surface of the substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FRANCIS P. SMITH whose telephone number is (571)270-3717. The examiner can normally be reached on Monday through Friday 7:30 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mikhail Kornakov can be reached on (571)272-1303. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FPS

/Michael Kornakov/
Supervisory Patent Examiner, Art Unit 4151